REMARKS

Claims 1-20 are pending in the application. Claims 1 and 11 have been amended by the present amendment. The amendments are fully supported by the application as originally filed (see, e.g., specification at page 4, line 24 to page 5, line 2).

Enclosed is a Letter to Official Draftsman accompanied by a new set of formal drawings incorporating the drawing correction filed on November 22, 2002, which was approved by the Examiner.

Applicants' claimed invention is directed to a semiconductor package and fabricating method in which a semiconductor chip is positioned above a plurality of passive devices, so as to reduce the space occupied on a substrate. As shown in FIG. 4C, the passive devices 3 are mounted on the substrate 2 and encapsulated by an insulative material 4. Then, a semiconductor chip 5 is stacked on the insulative material 4 and electrically connected to the substrate 2 by bonding wires 6 (see FIGS. 4D and 4E). As a result, the chip 5 is situated above the passive devices 3 without contacting the substrate. Subsequently, the chip 5 and bonding wires 6 are encapsulated by an encapsulant 7 (see FIG. 4E).

The above-described semiconductor package and fabricating method can yield significant benefits. Due to the vertical arrangement of the semiconductor chip and the passive devices, a reduced area of the substrate is occupied (see specification at page 4, lines 13-15), as compared to prior art packages in which passive devices are positioned beside a semiconductor chip. Moreover, the passive devices are encapsulated by the insulative material before mounting of the semiconductor chip, thereby preventing direct contact between the passive devices and bonding wires, and eliminating the occurrence of short circuits (see specification at page 4, line 24 to page 5, line 2).

Claims 1-5, 7, 10-15, 17, and 20 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,355,283 to Marrs et al. (hereinafter "Marrs") in view of U.S.

Patent 5,249,354 to Richman (hereinafter "Richman"). Claims 6, 8, 9, 16, 18, and 19 were rejected under 35 USC 103(a) as being unpatentable over "Marrs and Richman ... and further in view of" U.S. Patent 6,022,583 to Falcone et al. (hereinafter "Falcone"). These rejections are respectfully traversed, and for convenience are addressed together.

Marrs and Richman, whether taken alone or in combination, fail to teach or suggest a semiconductor package or fabricating method in which a semiconductor chip is positioned above pre-encapsulated passive devices and free of contact with the passive devices and substrate.

Marrs is directed to a BGA (ball grid array) package in which a plurality of vias are formed in a substrate to make electrical interconnection between a top surface and a bottom surface of the substrate (see column 3, lines 3-10). The vias are positioned within an area of the substrate where an encapsulant is formed. The vias are small concave depressions, instead of through holes, so as to eliminate drawbacks such as limited size of through holes formed by mechanical drilling, deformation of through holes, etc., as discussed in the Background section of Marrs (see column 2, lines 29-57). Marrs does not teach or suggest a semiconductor chip which is disposed **above** passive devices, such that the semiconductor chip is **free of contact** with the passive devices and the substrate, and does not address the issue of minimizing space occupied on the substrate.

With reference to FIG. 6 (cited in the Office Action), chip 601 is mounted on substrate 602 and electrically connected to the substrate 602 by bond wires 606. An encapsulant 603 encapsulates the chip 601 and bond wires 606; vias 607 in the substrate 602 are filled with an epoxy resin 609 (see column 7, lines 10-25). Marrs explicity states that "[p]assive components, such as resistors and capacitors, can also be mounted on the substrate" (column 2, lines 66-67). In other words, passive components optionally are included in the package of Marrs, and would be mounted on the substrate. However, Marrs does not teach or suggest that the semiconductor chip would be disposed above the passive components and free of contact with the passive components and the substrate, as required in claims 1 and 11 of the Applicants' invention.

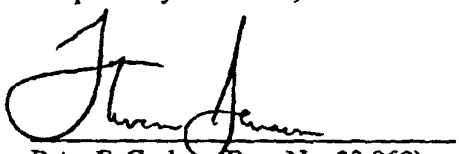
It is apparent from Marrs that, if passive components are included in a package, they would be mounted on a substrate beside the semiconductor chip. Marrs does not teach or suggest disposing the semiconductor chip **above** passive devices, such that the semiconductor chip is **free of contact** with the passive devices and the substrate.

Richman fails to remedy the deficiencies of the Marrs reference. Richman is directed to a lead-frame-based package which allows a mounting pad to be made thinner than lead frame fingers, so as to reduce the thickness of the encapsulated package. In Richman, a chip 25 (and/or other active/passive component(s)) is attached to a mounting pad 22, and electrically connected to lead frame fingers 21 by wires 23 (see FIG. 2, as cited in the Office Action). However, there is no teaching or suggestion in Richman for disposing a semiconductor chip above the passive components and free of contact with the passive components and the substrate, as required in claims 1 and 11 of the Applicants' invention.

Therefore, the combination of Marrs in view of Richman cannot anticipate or otherwise render obvious the Applicant's claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 11 have been amended as follows:

1. (Amended) A fabricating method of a semiconductor package, comprising the steps of:

providing a substrate having a device-mounting region [predefined within a chip-mounting region] on a surface of the substrate, and a wire bonding region predefined around the device-mounting region for forming a plurality of bonding fingers thereon;

mounting a plurality of passive devices on the device-mounting region;

using an insulative material for encapsulating the passive devices;

disposing a semiconductor chip on a surface of the insulative material above the passive devices, such that the semiconductor chip is free of contact with the passive devices and the substrate;

providing a plurality of bonding wires for electrically connecting the semiconductor chip to the bonding fingers of the substrate;

forming an encapsulant for encapsulating the semiconductor chip and the bonding wires; and

providing a plurality of conductive members for electrically connecting the substrate to an external device.

11. (Amended) A semiconductor package, comprising:

a substrate having a device-mounting region predefined on a surface of the substrate, and a wire bonding region predefined around the device-mounting region for forming a plurality of bonding fingers thereon;

a plurality of passive devices attached to the device-mounting region;

an insulative material for encapsulating the passive devices;

a semiconductor chip disposed on a surface of the insulative material above the passive devices, such that the semiconductor chip is free of contact with the passive devices and the substrate;

a plurality of bonding wires for electrically connecting the semiconductor chip to the bonding fingers of the substrate;

an encapsulant for encapsulating the semiconductor chip and the bonding wires; and

a plurality of conductive members for electrically connecting the substrate to an external device.